REMARKS

The application includes claims 2, 4-8, 10, 12-13, and 20-33 prior to entering this amendment.

The examiner withdrew the allowability of claim 1.

The examiner objected to claims 2 and 26 for informalities.

The examiner rejected claims 2, 4, 10 and 12 under 35 U.S.C. § 103(a) as being unpatentable over Birkett (U.S. Patent No. 6,977,976) in view of Mohindra (U.S. Patent No. 7,110,734) and Moriwaki (U.S. Patent No. 5,014,056).

The examiner rejected claims 5-8 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Birkett in view of Mohindra, Moriwaki, and Sacca (U.S. Patent No. 5,680,075).

The examiner rejected claims 20, 26, and 31-33 under 35 U.S.C. § 103(a) as being unpatentable over Birkett in view of Moriwaki.

The examiner rejected claim 21 under 35 U.S.C. § 103(a) as being unpatentable over Birkett in view of Moriwaki and Liang (U.S. Patent No. 7,145,934).

The examiner rejected claims 22-25, 27-30 under 35 U.S.C. § 103(a) as being unpatentable over Birkett in view of Moriwaki and Mohindra.

The applicant amends claims 2, 4-5, 10, 13, 20, 22-23, and 26 and cancels claims 24-25 and 27-33 without prejudice. The applicant had previously canceled claims 1, 3, 9, 11, and 14-19.

The application remains with claims 2, 4-8, 10, 12-13, 20-23, and 26 after entering this amendment.

The applicant does not add new matter and requests reconsideration in view of the following remarks.

Claim Rejections Under § 103

Claim 2 recites *generating at least one digital counter signal responsive to the differences between the detected I and Q signal and at least one reference signal, generating a control signal by multiplexing the at least one counter signal with the reference signal,* and *controlling the respective I and Q VGAs with the control signal.*

Claim 10 recites the following:

where the ADC comprises:

i. a multi-level comparator to compare the digital detected I and Q output signal to at least one reference signal; and

ii. a logic circuit to generate at least one digital counter signal responsive to the multi-level comparator; and

where the digital engine comprises:

i. an up/down counter to generate an up/down counter signal responsive to the at least one digital counter signal; and

ii. a multiplexer to generate a control signal that digitally adjusts the respective I and Q VGAs by multiplexing the up/down counter signal with the at least one reference signal.

Claims 20 and 26 recite similar language.

In rejecting the previously recited *digitizing the detected I and Q signal* and *adjusting, with the associated control signal, the respective I and Q VGAs*, the examiner indicates that Birkett discloses the language when he discloses "the nature of the signals in and out of block 65."[1] Further, the examiner indicates that Birkett discloses the recited adjusting because "part of the digitizing involves the detected signal to be compared with a reference level...where comparison in the digital domain is used."[2] But Birkett's error amplifier 65 is an op-amp "whereby both inputs and outputs are analog. However, if the VGA's are digitally controlled, then the error amplifier 65 may be constructed using digital logic, with inputs and outputs being digital in nature."[3] That is the amplifier 65 receives digital inputs and generates digital outputs if the VGAs are digitally controlled. The amplifier 65 receives analog input and generates analog outputs if the VGAs are analog controlled. Birkett does not disclose that its amplifier 65 digitizes anything, much less the output of integrator d as it must to disclose the recite *generating at least one digital counter signal*. Moreover, the amplifier 65 provides the output k of the integrator d to the VGAs 43I and 43Q and the RSSI estimating circuit 32.[4] The output k therefore directly controls the VGAs 43I and 43Q. If the examiner identifies the output k as disclosing the recited digitized detected I and Q signal, the output k cannot also disclose differences between the digitized I and Q signals and the reference signal. If the examiner is

[1] Office action dated 10/30/2007, page 4.
[2] Id.
[3] Birkett, column 9, lines 54-59.
[4] See, e.g., Birkett, figures 2 and 4a.

suggesting the output k discloses the recited control signal, the output k cannot also disclose the digitized I and Q signal and a reference signal.

In rejecting the previously recited *receiving in an analog to digital converter (ADC).... comparing the detected I and Q signal to a reference signal, and generating digital up/down and count/hold control signals*, the examiner indicates that Moriwaki discloses an ADC 12 that compares the input signal to a reference signal and generates digital up/down and count/hold signal.[5] The examiner identifies the motivation to combine Birkett and Mohindra with Moriwaki "so that the detected I and Q signal of Birkett et al., is digitized as taught by Moriwaki in a fast and high resolution A/D converter..."[6] The claims, as amended, however, recite *generating at least one digital counter signal responsive to the differences between the detected I and Q signal and at least one reference signal, generating a control signal by multiplexing the at least one counter signal with the reference signal, and controlling the respective I and Q VGAs with the control signal.* Moriwaki's ADC 12 does not generate at least one counter signal as required by the claim. Rather, the ADC 12 generates digital bits D0-D10, providing the MSB to the U/D input of the Up/Down counter 20. If the examiner considers the bits D0-D10 as disclosing the recited the at least one digital counter signal, then the bits D0-D10 must be multiplexed to disclose the recited control signal. If the examiner considers the 17-bit output of the Up/Down counter 20 as disclosing the recited at least one counter signal, then that 17 bit output must be multiplexed to generate the control signal. Neither situation is disclosed in or obvious in view of Moriwaki.

Claim 2 further recites *passing the respective I and Q output signals through respective high pass filters (HPFs).* The examiner acknowledges that Birkett does not disclose the recited *passing* but proposes that Mohindra discloses passing the I and Q signals through the channel filters 24 and 25 motivated by the need to remove residual DC errors.[7]

Importantly, even if Mohindra's filters 24 and 25 operated as indicated by the examiner, Birkett would have no need to add them to his circuit "to remove (residual) DC errors." This is because Birkett's AGC stages 29i to 29n include DC compensation circuits 46I and 46Q that "detect the dc output of VGA's 43I and 43Q and feed back a negative voltage to adders 42I and

[5] Office action dated 10/30/2007, page 6.
[6] Id.
[7] Office action dated 10/30/2007, page 5.

42Q in order to remove the dc offset on the input signal before the controller 44 estimates the input signal ac levels."[8]

Although Mohindra's channel filters 24 and 25 operate on the signals output from the capacitors 22 and 23, they do not do so for removing the residual DC errors as the examiner indicates. Rather, the capacitors 22 and 23 and filters 24 and 25 form part of an AC coupler,[9] controlled by the state machine 9 so as to change the AC coupling frequency from 10MHz to 500 KHz.[10] "Temporary AC coupling is used to remove DC offsets that could otherwise saturate the receiver outputs due to the large gain the base band paths from the down converters outputs [sic] outputs to the I and Q outputs."[11] The examiner appears to confuse the function of the filters 24 and 25 with that of the DSP 30. It is the DSP 30 that "computes the DC offsets in the I and Q remaining parts of the signal. The average values of the I and Q signals are calculated by the DSP 30. The computed average DC offsets should be then subtracted from their respective signals for the rest of the packet. ... After this subtraction, a first order high pass filtering should be done on the following I and Q signals digitally by the DSP 30, which represents step 4 of the preferred embodiment."[12]

[8] Birkett, column 8, lines 47-51.
[9] Mohindra, column 3, lines 20-23.
[10] Mohindra, column 3, lines 30-33.
[11] Mohindra, column 3, lines 63-67.
[12] Mohindra, column 5, lines 2-11.

Conclusion

For the above reasons, the applicant requests reconsideration and allowance of the remaining claims. The applicant encourages the examiner to telephone the undersigned at (503) 224-2170 if it appears that an interview would be helpful in furthering prosecution.

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Respectfully submitted,

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